As of Oct. 22, 2014, our group's status of our processor design is as follows:

Milestone 3 complete, including the following:

* A complete block diagram of the datapath
* Descriptions of each control signal used in the datapath
* Unit tests for each component in the datapath, and integration tests for the datapath as a whole
* Xilinx implementation of some of the datapath components
  + Register File complete – testing next week
  + Sign extender started – testing next week
  + ALU complete – testing next week